**DSD Final Project Scores**

**1. BrPred**

(1) Total execution cycles of given I\_mem\_BrPred:

截圖:

(2) Total execution cycles of given I\_mem\_hasHazard:

截圖:

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um2)

**2. Compressed instructions**

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um2)

截圖:

(2) Total Simulation Time of given I\_mem\_compression: (ns)

截圖:

(3) Area\*Total Simulation Time: (um2 \* ns)

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

**3. Q\_sort**

(1) Area: (um2)

截圖:

(2) Best Total Simulation Time : (ns)

(either using compressed or uncompressed instructions)

截圖:

(3) Area\*Total Simulation Time: (um2 \* ns)

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)